ABSTRACT

A method of inspecting full-chip mask data to locate layout pattern design induced defects and weak points that cause functional failure or performance degradation for integrated circuits (ICs) manufactured in subwavelength technology. Given the pre-OPC integrated circuit design layout data, the method of present invention refers to available post-OPC data or generates post-OPC data condition to do the inspection based on the modeling of integrated circuit wafer patterning. Build-in direct checks of specified electrical functional defects and a multilayer pattern-centric approach are used to improve the accuracy and performance. A technique of adaptive search is used to speed up the critical dimension search during the process of optical proximity correction data verification. A defect synthesis capability is supplied for defect disposition to facilitate systematic correction and prevention of the defects in integrated circuit layout design.